

LB1845

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{BB} = 38\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{REF} = 5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Output Block]						
Output stage supply voltage	$I_{BB\text{ ON}}$			12	16	mA
	$I_{BB\text{ OFF}}$			0.7	0.9	mA
Output saturation voltage 1	$V_{O(\text{sat})1}$	$I_O = +1.0\text{ A sink}$		1.2	1.4	V
	$V_{O(\text{sat})2}$	$I_O = +1.5\text{ A sink}$		1.4	1.7	V
	$V_{O(\text{sat})3}$	$I_O = -1.0\text{ A source}$		1.1	1.3	V
	$V_{O(\text{sat})4}$	$I_O = -1.5\text{ A source}$		1.3	1.6	V
Output leakage current	$I_{O(\text{leak})1}$	$V_O = V_{BB}\text{ sink}$			50	μA
	$I_{O(\text{leak})2}$	$V_O = 0\text{ V source}$	-50			μA
Sustained output voltage	$V(\text{sus})$	*	45			V
[Logic Block]						
Logic supply current	$I_{CC\text{ ON}}$	$I_O = 0.8\text{ V}, I_1 = 0.8\text{ V}$		19.5	25.3	mA
	$I_{CC\text{ OFF}}$	$I_O = 2.4\text{ V}, I_1 = 2.4\text{ V}$		15.5	20.1	mA
Input voltage	V_{IH}		2.4			V
	V_{IL}				0.8	V
Input current	I_{IH}	$V_{IH} = 2.4\text{ V}$			10	μA
	I_{IL}	$V_{IL} = 0.8\text{ V}$	-10			μA
Current control threshold voltage	V_{REF}/V_{SENSE}	$I_O = 0.8\text{ V}, I_1 = 0.8\text{ V}$	9.5	10	10.5	
		$I_O = 2.4\text{ V}, I_1 = 0.8\text{ V}$	13.5	15	16.5	
		$I_O = 0.8\text{ V}, I_1 = 2.4\text{ V}$	25.5	30	34.5	
Thermal shutdown temperature	T_S			170		$^\circ\text{C}$

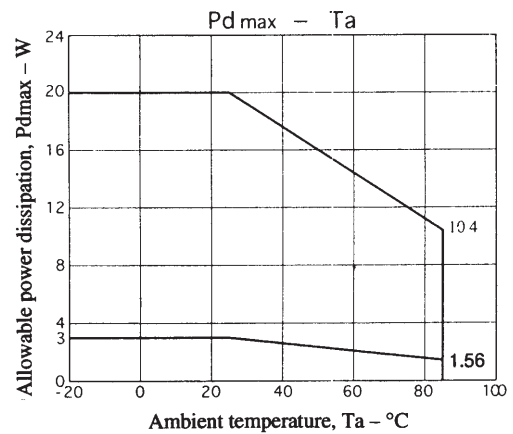
Note: *Design guaranteed value

Truth Table

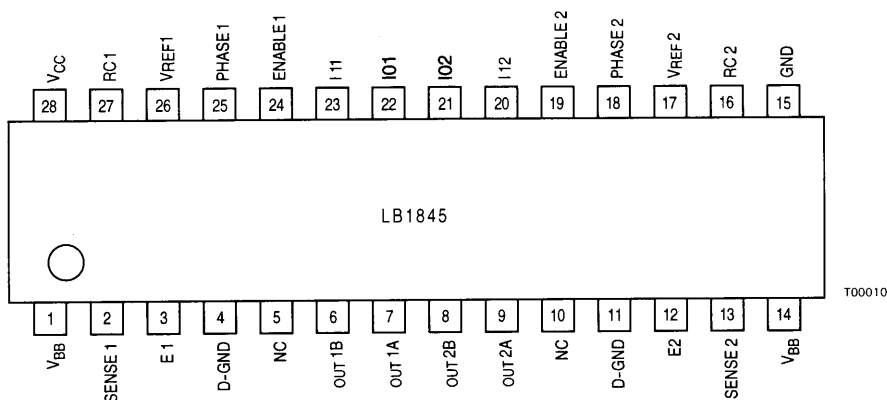
ENABLE	PHASE	OUT A	OUT B
L	H	H	L
L	L	L	H
H	—	OFF	OFF

I_0	I_1	Output current
L	L	$V_{REF} / (10 \times R_E) = I_{OUT}$
H	L	$V_{REF} / (15 \times R_E) = I_{OUT} \times 2/3$
L	H	$V_{REF} / (30 \times R_E) = I_{OUT} \times 1/3$
H	H	0

Note: Outputs go off when ENABLE is high or in the $I_0 = I_1 = \text{high state}$.

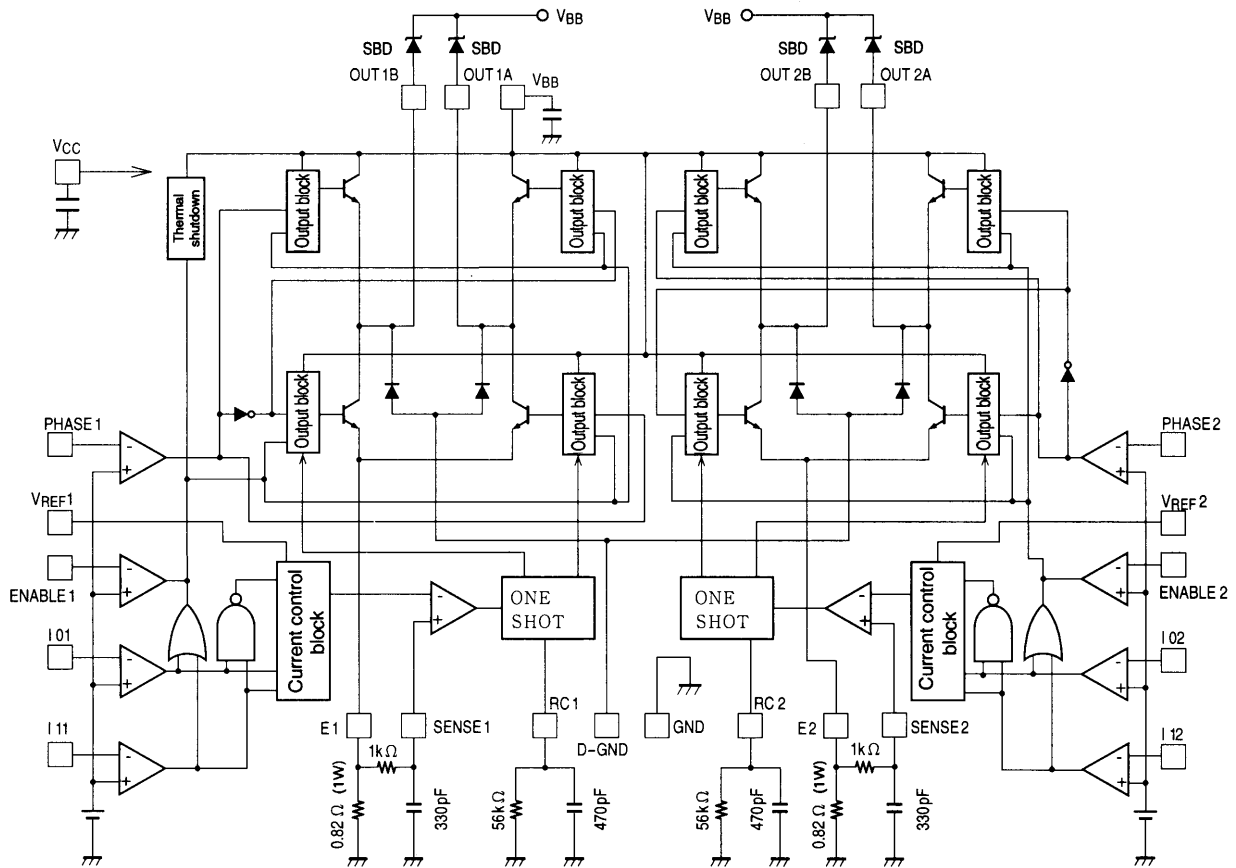


Pin Assignment



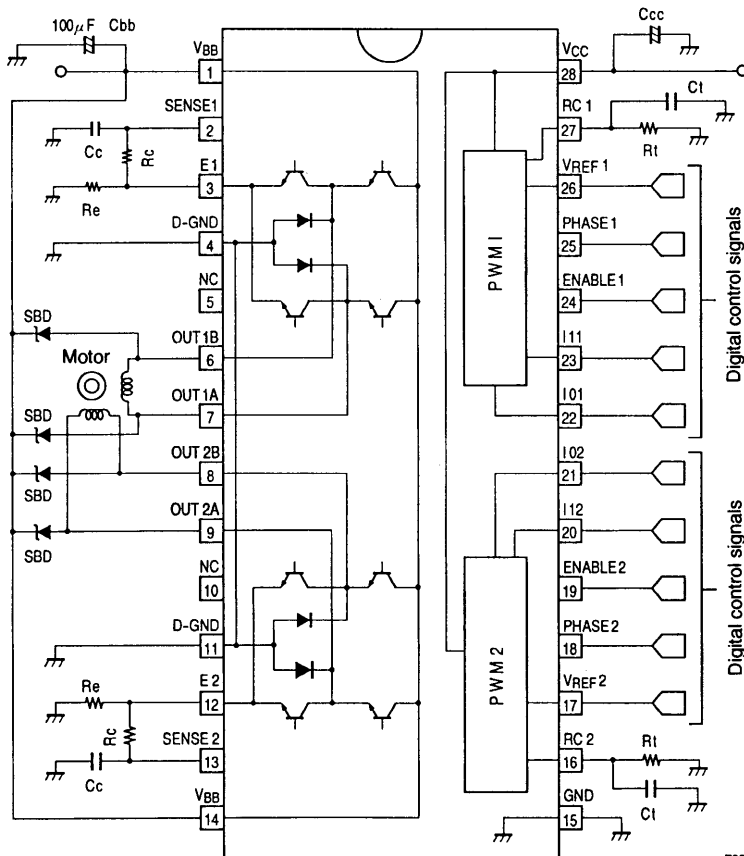
Top view

Block Diagram



T00011

Application Circuit Diagram



Off time setting values
 $t_{off} \approx C1R1$

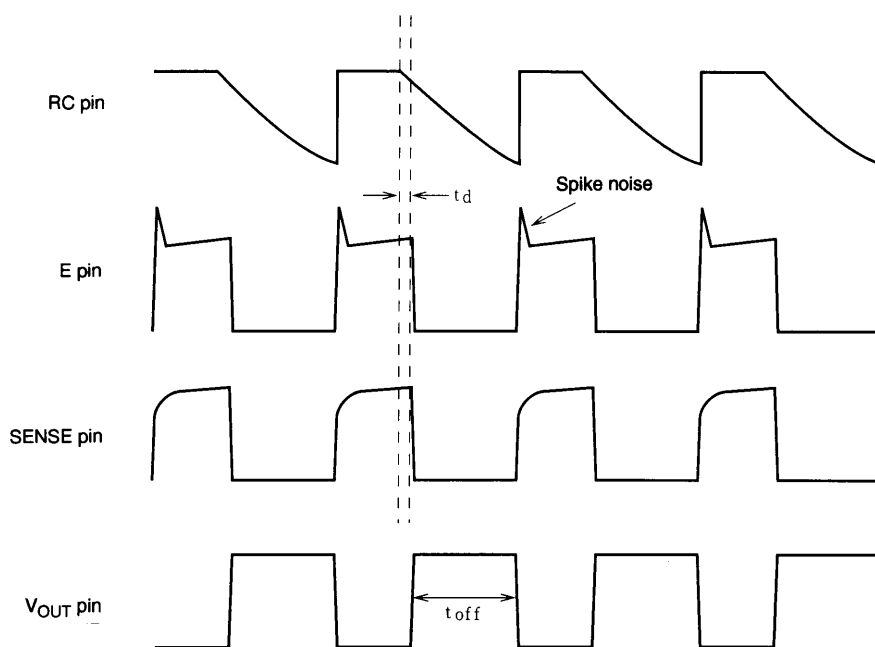
- Re = 0.82 Ω (1W)
- VREF = 5V
- Rt = 56 kΩ
- Ct = 470 pF
- Rc = 1 kΩ
- Cc = 330 pF
- Cbb = 100 μF

T00012

Pin Functions

Pin no.	Pin	Function
1, 14	V _{BB}	Output stage power-supply voltage
2	SENSE1	Set current detection pins.
13	SENSE2	Connect these pins, fed back through noise filters, to E1 and E2.
3	E1	The set current is controlled by the resistors R _e inserted between these pins and ground.
12	E2	
4, 11	D-GND	Internal diode anode connection
6	OUT 1B	Outputs
7	OUT 1A	
8	OUT 2B	
9	OUT 2A	
15	GND	Ground
27	RC1	Used to set the output off time for the switched output signal.
16	RC2	The fixed off times are set by the capacitors and resistors connected to these pins. $t_{off} = CR$.
26	V _{REF1}	Output current settings
17	V _{REF2}	The output current is determined by the voltage (in the range 1.5 to 7.5 V) input to these pins.
25	PHASE1	Output phase switching inputs.
18	PHASE2	High-level input: OUT A = high, OUT B = low Low-level input: OUT A = low, OUT B = high
24	ENABLE1	Output on/off settings
19	ENABLE2	High-level input: output off Low-level input: output on
22, 23	I01, I11	Digital inputs that set the output current
21, 20	I02, I12	The output currents can be set to 1/3, 2/3, or full by setting these pins to appropriate combinations of high and low levels.
28	V _{CC}	Logic block power supply

Timing chart for pin switching operations during PWM drive



T00013

Figure 1 Switching Waveforms

t_{off} : Output off time. Determined by external capacitor and resistor C_t and R_t . ($t_{off} = C_t \times R_t$)

t_d : Delay time between the point the set current is sensed at the SENSE pin and the point the output turns off.

Usage Notes

1. External diode

Since this IC adopts a system based on lower side transistor switching drive, an external diode for the regenerative current that occurs during switching is required between V_{BB} and V_{OUT} . Use a Schottky barrier diode with a low feedthrough current.

2. Noise filters

Since spike noise (see Figure 1) occurs when switching to the on state due to the external diode's feedthrough current, applications must remove noise from the SENSE pin with a noise filter (C_c , R_c) between the E pin and the SENSE pin. However, note that if the values of C_c and R_c are too large, the SENSE voltage rise will be slowed, and the current setting will be shifted towards a higher current level.

3. V_{REF} pin

It is possible to change the output current continuously by continuously changing the V_{REF} pin voltage. However, this voltage cannot be set to 0 V. The V_{REF} pin input impedance is 26 k Ω ($\pm 30\%$) when V_{REF} is 5 V. Since this pin is used to set the output current, applications must be designed so that noise does not appear on this pin's input.

4. GND pin

Since this IC switches large currents, care must be taken to avoid ground loops when the IC is mounted in the application. The section of the PCB that handles large currents should be designed with a low-impedance pattern, and must be separated from the small signal sections of the circuit. In particular, the ground for the sense resistor R_e must be as close as possible to the IC ground.

5. Operation in hold mode

There are cases where a current somewhat larger than the current setting may flow in hold mode (light load mode). Since this IC adopts a lower side switching, lower side sense system, the emitter voltage falls and the sense voltage goes to 0 when the switching state goes to off. The circuit then always turns the output on after the toff period has elapsed. At this time, due to the light load, the existence of the time t_d , and the fact that the output goes on even if the output current is higher than the set current, the output current will be somewhat higher than the set current. Applications should set the current setting somewhat lower than required if this occurs.

6. Function for preventing the upper and lower outputs being on at the same time

This IC incorporates a built-in circuit that prevents the through currents that occur when the phase is switched. The table lists the output on and off delay times when PHASE and EANBLE are switched.

		Sink side	Source side
When PHASE is switched	On delay time	10 μ s	9 μ s
	Off delay time	1.5 μ s	3 μ s
When ENABLE is on	On delay time	9 μ s	9 μ s
	Off delay time	1.5 μ s	6.5 μ s

7. 1-2 phase excitation and the double 1-2 phase excitation control sequence

To reduce the vibration that occurs when the motor turns, this IC supports 1-2 phase excitation and double 1-2 phase excitation by using the output current setting digital input pins I0 and I1 without changing the V_{REF} pin voltage. Tables 1 and 2 list that control sequence, and Figure 2 and Figure 3 present the composite vector diagram for this sequence.

Noise filters

Table 1 [1-2 phase excitation] 1/2 step

ENABLE1 = ENABLE2 = 0

No.	Phase A				Phase B			
	PH1	I11	I01	Current value	PH2	I12	I02	Current value
0	0	0	0	1	*	1	1	0
1	0	0	1	2/3	0	0	1	2/3
2	*	1	1	0	0	0	0	1
3	1	0	1	2/3	0	0	1	2/3
4	1	0	0	1	*	1	1	0
5	1	0	1	2/3	1	0	1	2/3
6	*	1	1	0	1	0	0	1
7	0	0	1	2/3	1	0	1	2/3

Table 2 [Double 1-2 phase excitation] about 1/4 step

ENABLE1 = ENABLE2 = 0

No.	Phase A				Phase B			
	PH1	I11	I01	Current value	PH2	I12	I02	Current value
0	0	0	0	1	*	1	1	0
1	0	0	0	1	0	1	0	1/3
2	0	0	1	2/3	0	0	1	2/3
3	0	1	0	1/3	0	0	0	1
4	*	1	1	0	0	0	0	1
5	1	1	0	1/3	0	0	0	1
6	1	0	1	2/3	0	0	1	2/3
7	1	0	0	1	0	1	0	1/3
8	1	0	0	1	*	1	1	0
9	1	0	0	1	1	1	0	1/3
10	1	0	1	2/3	1	0	1	2/3
11	1	1	0	1/3	1	0	0	1
12	*	1	1	0	1	0	0	1
13	0	1	0	1/3	1	0	0	1
14	0	0	1	2/3	1	0	1	2/3
15	0	0	0	1	1	1	0	1/3

Composite Vector Diagram

[1-2 phase excitation]

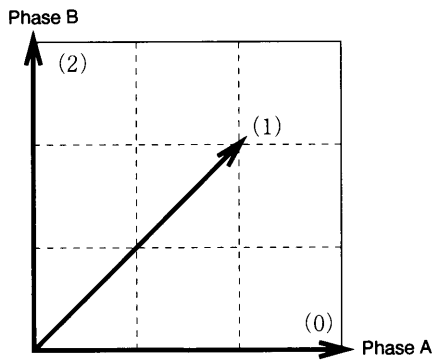


Figure 2 Composite Vector Diagram for the Sequence in Table 1 (1/4 cycle)

[Double 1-2 phase excitation]

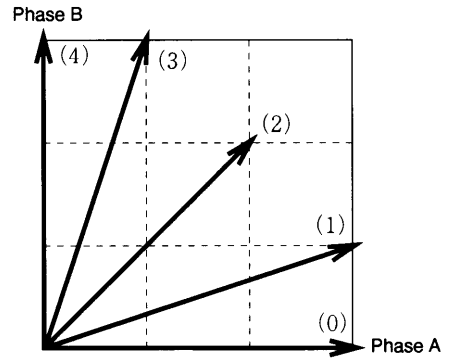
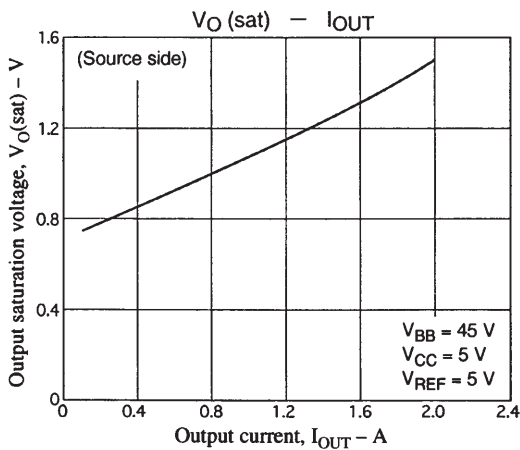
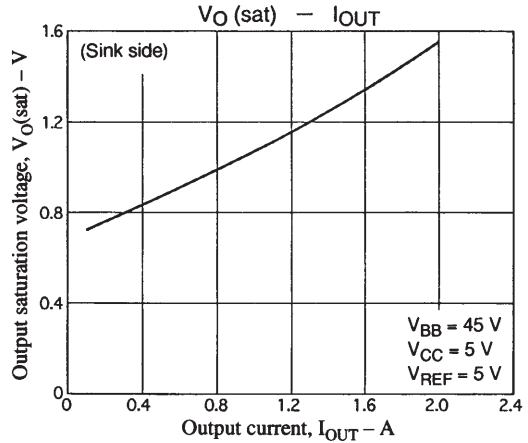
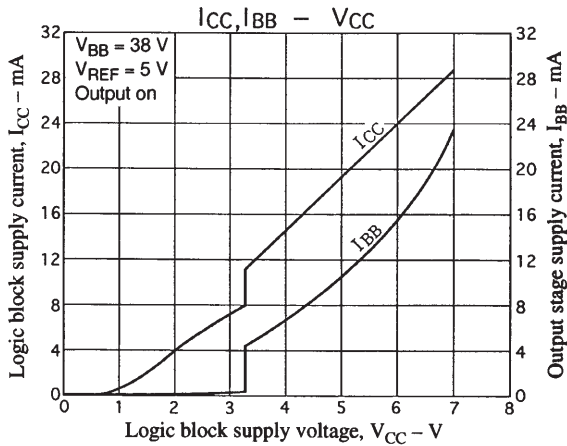
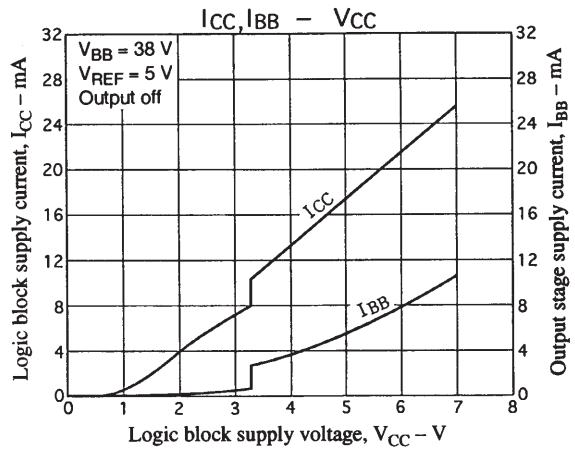
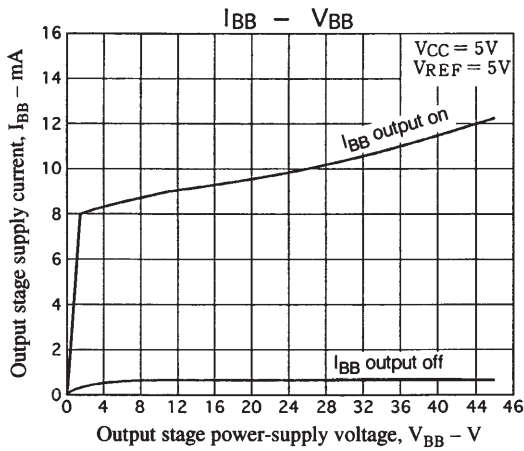


Figure 3 Composite Vector Diagram for the Sequence in Table 2 (1/4 cycle)



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